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09/458,506	12/09/1999	TAE-GYOUNG KANG	5484-53	8916

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/458,506	Applicant(s) KANG, TAE-GYOUNG
	Examiner ori nadav	Art Unit 2811

-- The MAILING DATE of this communication appears on the cover sh t with the correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 April 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *14-25 and 29-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *14-25 and 29-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/23/2002 has been entered. An action on the RCE follows.

2. The amendment filed on 2/20/2002 has been entered.

Claim Objections

3. Claims 14-25 and 29-39 are objected to because of the following informalities: Although the claimed limitations of a plurality of transistor gates having identical gaps therebetween without intervening transistor gates therebetween, as recited in claims 14, 18, 22, 29, 33 and 36, and a plurality of dummy gates having identical gaps therebetween without intervening dummy gates therebetween, as recited in claims 14, 18, 22, 29 and 33, are unclear, it is understood that applicant wanted to overcome the rejection recited in previous office action by introducing the limitations of a plurality of transistor gates having identical gaps therebetween without intervening dummy gates therebetween, and a plurality of dummy gates having identical gaps therebetween

without intervening transistor gates therebetween, respectively . Appropriate correction is required.

4. Claim 14 recites the limitation "the adjacent transistor gates" in lines 7-8. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

5. Claim 22 recites the limitation "the adjacent gates" in line 8. There is insufficient antecedent basis for this limitation in the claim. Appropriate correction is required.

6. The claimed limitation of "the plurality of first gates", as recited in claim 33, line 10, should read "the plurality of first transistor gates". Appropriate correction is required.

7. The claimed limitation of "the plurality of second gates", as recited in claim 33, line 14, should read "the plurality of second transistor gates". Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

9. Claims 38-39 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Independent claim 36 recites a plurality of transistor gates having a first dimension and a variable second dimension, wherein the plurality of transistor gates have substantially identical first and second dimensions. Dependent claim 37 recites the first dimension being a transistor gate length, and dependent claim 38 recites the second dimension being a transistor gate width. Thus, claim 38 recites plurality of transistor gates having substantially identical length and width dimensions. There is no support in the specification as filed for plurality of transistor gates having substantially identical length and width dimensions, as recited in claim 38.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 14, 16-18, 20-22, 24-25 and 29-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Nagamine (5,534,724) and Bothra et al. (6,020,616).

Regarding claims 14, 18, 22, 29, 33, 34 and 36, APA teaches in figure 10 and related text pages (1-3 and 5-7) a semiconductor device comprising active regions of two or more adjacent transistors having at least more than one first and second electrodes ME2 (figure 9), a plurality of transistor gates P2G (figure 5) disposed between more than one first and second electrodes ME2 of those active regions respectively, wherein two or more gates P2G, P3G are of a predetermined width and length at a substantially identical gap between ones of the adjacent transistor, without intervening transistor and dummy gates therebetween.

APA does not teach a substrate and a plurality of dummy gates having a predetermined width and length between and outside ones of the adjacent transistors at a substantially identical gap between adjacent ones of the dummy gates, without intervening transistor

and dummy gates therebetween, as that between the adjacent ones of the transistor gates on a substrate.

Nagamine teaches in figure 3 and related text a semiconductor device comprising a substrate (column 5, line 10), active regions 16 of two or more adjacent transistors having source and drain regions (column 4, lines 62-65), a plurality of transistor gates 10 on the substrate, wherein two or more gates 10 are of a predetermined width and length (figure 1) at a substantially identical gap between ones of the adjacent transistor gates (figure 4 and column 6, lines 19-24), without intervening transistor and dummy gates therebetween, on the substrate, and a plurality of dummy gates 20 having a predetermined width and length (figure 1) at a substantially identical gap between adjacent ones of the dummy gates (figure 4 and column 6, lines 19-24), without intervening transistor and dummy gates therebetween, as that between the adjacent ones of the transistor gates 10 on a substrate.

Bothra et al. teach in figure 3L and related text a plurality of dummy gates 226 (column 5, lines 35-60) having a predetermined width and length formed between and outside ones of the adjacent transistors 204.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form APA's device on a substrate wherein a plurality of dummy gates having a predetermined width and length are formed between and outside ones of the adjacent transistors, as taught by Bothra et al., and wherein the dummy gates

have substantially identical gap therebetween, without intervening transistor and dummy gates therebetween, as that between the adjacent transistor gates on the substrate, as taught by Nagamine, in order to support the device (by providing a substrate thereunder), to reduce the inductive noise of the device (by providing a plurality of dummy gates having a predetermined width and length between and outside ones of the transistors) and in order to simplify the processing steps of making the device (by providing a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates), respectively. The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates having a predetermined width and length between and outside adjacent transistors (figure 3L and column 2, lines 61-67), and by the teachings of Nagamine who points out the advantages of forming a plurality of dummy gates at a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates (column 2, lines 38-41),

Regarding claim 29, APA teaches in figure 5 active regions having source and drain regions P2S, P2D, and a portion other than the active region, wherein gates P2G, P3G are disposed between the source and drain regions P2S, P2D and P3S, P3D, respectively. Note that the claimed limitation of a second gap being substantially identical to a first gap was addressed in previous paragraph.

Regarding claims 30, 31 and 33, APA teaches in figure 5 a first region (the region above line 62) having plurality of first active regions each having source and drain regions P2S, P2D and P3S, P3D, respectively, and a first portion other than the first active regions, a second region (the region below line 62) having plurality of second active regions each having source and drain regions N4S, N4D and N3S, N3D, respectively, and a second portion other than the first active regions, first and second transistor gates P2G, P3G and N4G, N3G, respectively, are disposed between the source and drain, respectively, and having a first gap therebetween, and a first metal ME2 (figure 9) connected to the source and drain regions by a plurality of contacts 70, and a second metal 64 connected to a first part of the first metal to supply voltage.

Regarding claim 36, APA teaches in figure 5 a plurality of transistor gates P2G having a first dimension L and a plurality of transistor gates P3G having a variable second dimension L, wherein the plurality of transistor gates P2G, P3G have substantially identical first and second dimensions L (page 6, lines 22-23).

Regarding claims 16, 20 and 24, APA teaches in figure 5 at least more than one gate P2G, P3G of a plurality of transistors respectively have common terminals

Regarding claims 17, 21 and 25, APA does not teach a plurality of dummy gates commonly connected. Bothra et al. teach in figure 3L a plurality of dummy gates 226 commonly connected. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the plurality of dummy gates commonly connected, as taught by Bothra et al., in APA's device in order to suppress the inductive noise of the device. The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a plurality of dummy gates commonly connected (column 5, lines 40-50),

Regarding claim 32, APA teaches in figure 10 a second metal ME3 connected to a second part of the first metal to supply ground voltage (page 7, lines 17-21). APA does not teach a plurality of dummy gates commonly connected to a second part of the first metal to supply ground voltage. Bothra et al. teach in figure 3L a plurality of dummy gates 226 commonly connected to a ground voltage (column 5, lines 40-50). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the plurality of dummy gates commonly connected to a second part of the first metal to supply ground voltage, as taught by Bothra et al. and APA, in APA's device in order to suppress the inductive noise of the device. The combination is motivated by the teachings of Bothra et al. who point out the advantages of forming a

plurality of dummy gates commonly connected to a ground voltage (column 5, lines 40-50),

Regarding claim 34, the claimed limitation of a second gap being substantially identical to a first gap was addressed in detail on pages 6-7.

Regarding claim 35, APA teaches in figure 10 a second metal ME3 connected to a second part of the first metal to supply ground voltage (page 7, lines 17-21).

Regarding claim 37, APA teaches in figure 5 a first dimension L being a transistor gate length.

12. Claims 15, 19 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Nagamine and Bothra et al., as applied to claims 14, 18, 22 above, and further in view of Hansch et al. (6,174,741).

Regarding claims 15, 19 and 23, APA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as applied to claims 14, 18, 22 above, except stating that the length of the dummy gates is substantially the same as that of the transistor gates. Hansch et al. teach in figures 3B and 4 the length of dummy gates DG, DGL is substantially the same as that of the transistor gates G, GL, respectively.

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the length of the dummy gates substantially the same as that of the transistor gates, as taught by Hansch et al., in the device of APA, Nagamine and Bothra et al. in order to simplify the processing steps of making the device by forming the transistor gates and the dummy gates with the same width and length..

13. Claims 38-39, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA), Nagamine and Bothra et al., as applied to claims 36 and 37 above, and further in view of Neugebauer (5,748,835).

Regarding claim 38, APA, Nagamine and Bothra et al. teach substantially the entire claimed structure, as applied to claims 36 and 37 above, except a second dimension being a transistor gate width, i.e. a plurality of transistor gates having substantially identical length and width dimensions.

Neugebauer teaches a plurality of transistor gates having substantially identical length and width dimensions (column 13, lines 6-8).

it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of transistor gates having substantially identical length and width dimensions as taught by Neugebauer, in the device of APA,

Nagamine and Bothra et al., in order to minimize the error of each of the channel coupled semiconductors when using the device in channel coupled feedback circuits.

Regarding claim 39, the claimed limitation of adjacent ones of the plurality of transistor gates and of the plurality dummy gates are of substantially identical gap between gates, was addressed in detail on pages 6-7.

Response to Arguments

14. Applicant's arguments with respect to claims 14-25 and 29-39 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference N is cited as being related to a device comprising a plurality of dummy gates.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

May 16, 2002